Amendments to the Specification:

Please replace [Para 5] with the following amended paragraph:

[Para 5] As known by those skilled in the art, digital signal circuits are triggered by clocks to process and transmit sequential digital signals and to synchronize timing of function blocks. Due to the increasing complexity of digital signal circuits, parameters and functions of circuits require more careful design. Please refer to Fig.1 and Fig.2. Fig.1 and Fig.2 illustrate conventional digital signal circuits 10 of different implementation methods. As shown in Fig.1, to complete functions of ordinary digital signal circuits, the signal circuit 10 comprises a logic array 12, a plurality of flip-flops 14A and 14B, and a clock control circuit 16. The clock control circuit 16 generates a reference clock 18B according to a source clock 18A; the source clock 18A can be ~~generate~~ generated by the oscillator in the signal circuit 10, or be fed by other oscillation circuits outside the signal circuit 10. Each flip-flop 14A, 14B comprises an input port 13A, an output port 13B, and a clock port 15. Input port 13A receives input signals (as two different input data from two input ports), clock port 15 receives the triggering signal, and the flip-flops 14A, 14B, triggered by clocks of clock port 15, change output signals of output port 13B according to signals of input port 13A (as two different output data of two output ports). The rising edge of the clock signal from clock port 15 triggers flip-flop 14A, leading to data transition in the output signals of output port 13B while the falling edge of the clock signal from clock port 15 triggers flip-flop 14B, resulting in data transition in the output signals of output port 13B. The logic array 12 comprises several kinds of logic gates, such as AND gate 19A and OR gate 19B in Fig.1. Proper connection of input ports/output ports of flip-flops 14A and 14B as well as logic gates of logic array 12

facilitates implementation of different functions of digital signal circuits, such as adders, timers, state machines, etc. In addition, the signal circuit 10 comprises a plurality of output pads 22. For example, the signal circuit 10 can be enclosed in a package, with each output pad 22 being a pin extending outside the package. Thus, output signals of logic gates in logic array 12 or flip-flop output ports can be sent outside the signal circuit 10 by theses output pads 22. Output ports of the flip-flops and outputs of the logic gates in the logic array 12 are taken as data paths of output signals of the signal circuit 10, and each output port becomes a transmission medium of a data path of the signal circuit 10.

Please replace [Para 12] with the following amended paragraph.

[Para 12] In summary, in the signal circuit 10, there [[is]] <u>are</u> often logic operations between the reference clock and other signals, so that results of logic operations directly relate to timing of the reference clock. Even in some special circuits, such as a field programmable gate array, the clock cannot be output directly from output pads, but through a data path of a logic array and flip-flops. However, as discussed before, in the prior art, if the clock in the clock path directly performs logic operations, there will be much difficulty in operation and design of the circuits, so it is difficult for circuit designers to control clocks after logic operations.